CLAIMS

[1] A semiconductor integrated circuit device, comprising:

first to n-th shift registers;

first to n-th input terminals that receive data fed to the first to n-th shift registers;

a first switch that electrically connects and disconnects an output of a k-th shift register (where *k* is an integer such that $1 \leq k \leq n-1$) and an input of a k+1-th shift register;

a second switch that electrically connects and disconnects an input of the k+1-th shift register and a k+1-th input terminal that receives data to the k+1-th shift register; and

a selection signal input terminal that receives a selection signal for switching ON/OFF of the first switch and the second switch,

wherein, when the k-th shift register and the k+1-th shift register are used in a combined manner, the first switch is turned ON and the second switch is turned OFF by the selection signal, and

wherein, when the k-th shift register and the k+1-th shift register are used separately, the first switch is turned OFF and the second switch is turned ON by the selection signal.

[2] The semiconductor integrated circuit device of claim 1,

wherein there is provided an input driver between the k+1-th input terminal and the second switch, and

wherein there is provided an input driver inside the first shift register.

[3] The semiconductor integrated circuit device of claim 1,

wherein the first and second switches are transistor switches.

[4] A semiconductor integrated circuit device, comprising:

first to n-th shift registers;

first to n-th input terminals that receive data fed to the first to n-th shift registers; and

a switching control portion that performs, according to whether or not a k+1-th input terminal that receives data to a k+1-th shift register (where k is $1 \leq k \leq n-1$) is connected to an outside, switching control of whether an output of the k-th shift register and an input of the k+1-th shift register are connected together, or the k+1-th input terminal and an input of the k+1-th shift register are connected together,

wherein, when the switching control portion recognizes that the k+1-th input terminal is in an open state in which the k-th input terminal is not connected to the outside, an output of the k-th shift register and an input of the k+1-th shift register are connected together, and the k+1-th input terminal and an input of the k+1-th shift register are disconnected from one another, and

wherein, when the switching control portion recognizes that the k+1-th input terminal is connected to the outside and data is inputted thereto, an output of the k-th shift register and an input of the k+1-th shift register are disconnected from one another, and the k+1-th input terminal and an input of the k+1-th shift register are connected together.

[5] The semiconductor integrated circuit device of claim 4, further comprising:

a first switch that electrically connects and disconnects an output of the k-th shift register and an input of a k+1-th shift register; and

a second switch that electrically connects and disconnects an input of the k+1-th shift register and a k+1-th input terminal that receives data to the k+1-th shift register, and

wherein the switching control portion outputs a selection signal for switching ON/OFF of the first switch and the second switch.

[6] The semiconductor integrated circuit device of claim 5,

wherein there is provided, between the second switch and the k+1-th shift register, an input driver to which data inputted from the k+1-th input terminal is fed via the switching control portion, and

wherein there is provided an input driver inside the first shift register.

[7] The semiconductor integrated circuit device of claim 5,

wherein the first and second switches are transistor switches.

[8] The semiconductor integrated circuit device of claim 4,

wherein, when the data is in a form of a binary signal that shifts between a first voltage and a second voltage,

the switching control portion includes

a first resistance having one end connected to the k+1-th input terminal and the

other end to which the first voltage is applied,

a second resistance having one end connected to the k+1-th input terminal and the other end to which the second voltage is applied,

an external input detection circuit that receives a voltage at a node at which the first and second resistances and the k+1-th input terminal are connected together, the external input detection circuit that outputs a first signal when a voltage obtained by dividing the first and second voltages by the first and second resistances is detected, and outputs a second signal when the first or the second voltage is detected,

a first switch that turns ON when the first signal is outputted from the external input detection circuit, the first switch connected between an output of the k-th shift register and an input of the k+1-th shift register,

a first inverter that receives a voltage at a node at which the first and second resistances and the k+1-th input terminal are connected together,

a first transistor having a second electrode connected to the second voltage and a control electrode connected to an output of the first inverter,

a second transistor having an opposite polarity to the first transistor, the second transistor having a second electrode connected to the first voltage and a control electrode connected to an output of the first inverter,

a second switch having one end connected to a first electrode of the first transistor and the other end connected to an input of the k+1-th shift register, the second switch that turns ON when the second signal is inputted thereto from the external input detection circuit, and

a third switch having one end connected to a first electrode of the second transistor and the other end connected to an input of the k+1-th shift register, the third switch that turns ON when the second signal is inputted thereto from the external input detection circuit, and

wherein, when the first switch is turned ON, the second and third switches are turned OFF, and when the first switch is turned OFF, the second and third switches are turned ON.

[9] The semiconductor integrated circuit device of claim 8,

wherein the first voltage is higher than the second voltage,

wherein the external input detection circuit includes

a second inverter that receives a voltage at a node at which the first and second resistances and the k+1-th input terminal are connected together, and that outputs low level corresponding to the second voltage when a voltage that is higher than the voltage obtained by dividing the first and second voltages by the first and second resistances is inputted thereto,

a third inverter that receives a voltage at a node at which the first and second resistances and the k+1-th input terminal are connected together, and that outputs high level corresponding to the first voltage when a voltage that is lower than the voltage obtained by dividing the first and second voltages by the first and second resistances is inputted thereto,

a fourth inverter that receives an output of the third inverter, and

an exclusive OR circuit that receives outputs of the second and fourth inverters,

and

wherein, when high level is output from the exclusive OR circuit, the first switch turns OFF and the second and third switches turn ON, and when low level is outputted from the exclusive OR circuit, the first switch turns ON and the second and third switches turn OFF.